Design Example Report

Title	***100 W, Low Profile (11 mm), LLC DC-DC Converter Using HiperLCS™ LCS700HG***
Specification	380 VDC Input; 24 V, 3 A; 12 V, 2.32 A Outputs
Application	LCD TV
Author	Applications Engineering Department
Document Number	DER-282
Date	September 13, 2011
Revision	1.2

Summary and Features

- Very low parts count
  - Highly integrated solution for low parts count and small size
  - Low cost SMD (D-PAK) output diodes eliminates cost of heat sink and mounting
- High operating frequency (270 kHz) reduces size and cost
  - Enables use of ceramic output capacitors
  - Reduces size of transformer, low profile EFD30 transformer used
  - Burst Mode ensures no-load regulation
- High efficiency
  - >94% at 100% load, >93% at 50% load
  - Capacitive current sense for low power dissipation

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Important Notes:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. In addition, the transformer requires a suitable shroud to meet primary to core to secondary spacing.

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1 Important Notes

For proper operation, the board must be used with a bulk capacitor of at least 10 μF between the +380 V input and the input return placed directly across the terminals.

The board required an external bias supply of 12 V for operation. Do not apply a voltage greater than 15 V or IC damage will result.

This power supply has short-circuit protection, but no output overvoltage protection. Performing an overvoltage test by disabling the TL431 (U3) or optocoupler (U2) will cause the output voltage to rise sufficiently to break down the output Schottky rectifiers (D2-D3) and destroy them. Therefore this test should not be performed without adding overvoltage protection circuitry.

The burst mode feature may cause slightly higher ripple voltage at output typically under light load and high input voltage conditions. Burst mode -2[1] of the LCS700HG is selected for this design.

Soft-start performance can be optimized by selecting appropriate value of capacitance C3 depending on applicable specification.

This design uses surface mount Schottky diode rectifiers. Voltage de-rating requirements must be carefully evaluated for use of this design. Components with higher ratings should be substituted depending on de-rating requirements

[1] See HiperLCS data sheet for Burst-Mode operation detail.

2 Introduction

This document is an engineering report describing a 12 V / 24 V, 100 W LLC DC-DC resonant converter utilizing a LCS700HG integrated LLC control/power stage IC. This power supply is intended for use in an LCD TV with LED back light. The board requires +12 VDC and +380 VDC inputs.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

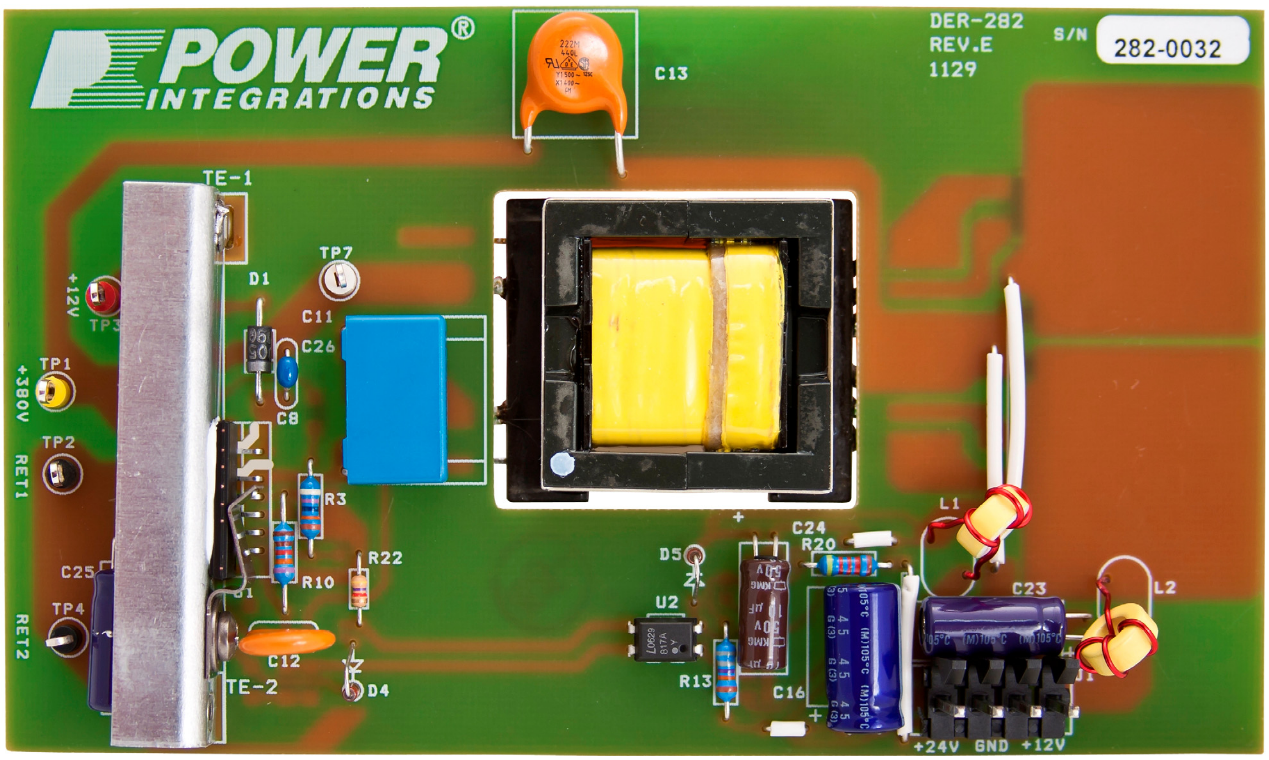

Figure 1 – Populated Circuit Board Photograph, Top View (L: 136.27 mm x W: 79.88 mm).

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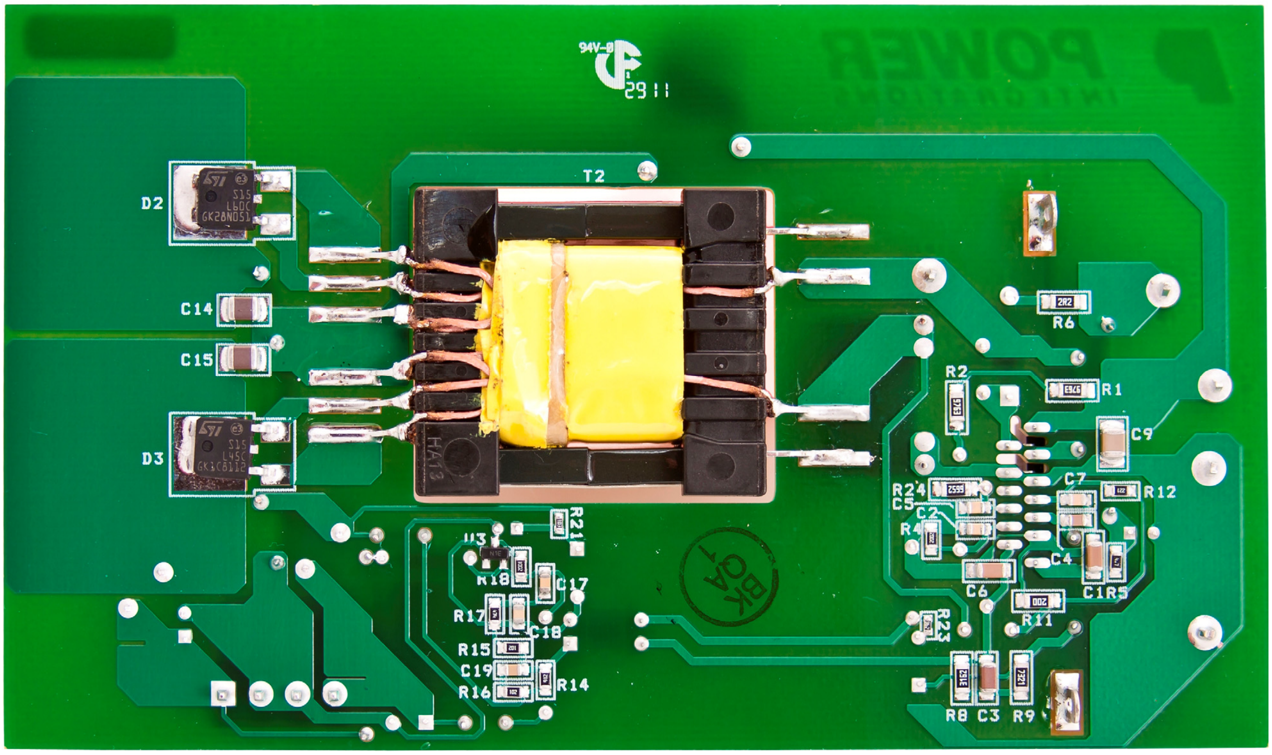

Figure 2 – Populated Circuit Board Photograph, Bottom View.

3 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	300	380	420	VDC	DC Input Only.
Output						
Output Voltage 1	V_{OUT1}	11.4	12	12.6	V	±5%
Output P-P Ripple Voltage 1	$V_{RIPPLE1}$			120	mV	20 MHz bandwidth
Output Current 1	I_{OUT1}	0.01	2.33	3.00	A	Total Load on Both Outputs ≤100 W
Output Voltage 2	V_{OUT2}	22.8	24	25.2	V	±5%
Output P-P Ripple Voltage 2	$V_{RIPPLE2}$			240	mV	20 MHz bandwidth
Output Current 2	I_{OUT2}	0.01	3.00	3.00	A	Total Load on Both Outputs ≤100 W
Total Output Power						
Continuous Output Power	P_{OUT}			100	W	
Peak Output Power	P_{OUT_PEAK}			100	W	
Efficiency						
20% Load	η	89.5	90		%	DC-DC Converter Target Efficiency, Measured at 25 °C, 380 VDC Input
50% Load	η	93.3	94		%	DC-DC Converter Target Efficiency, Measured at 25 °C, 380 VDC Input
100% Load	η	94	94.5		%	DC-DC Converter Target Efficiency, Measured at 25 °C, 380 VDC Input

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4 Schematic

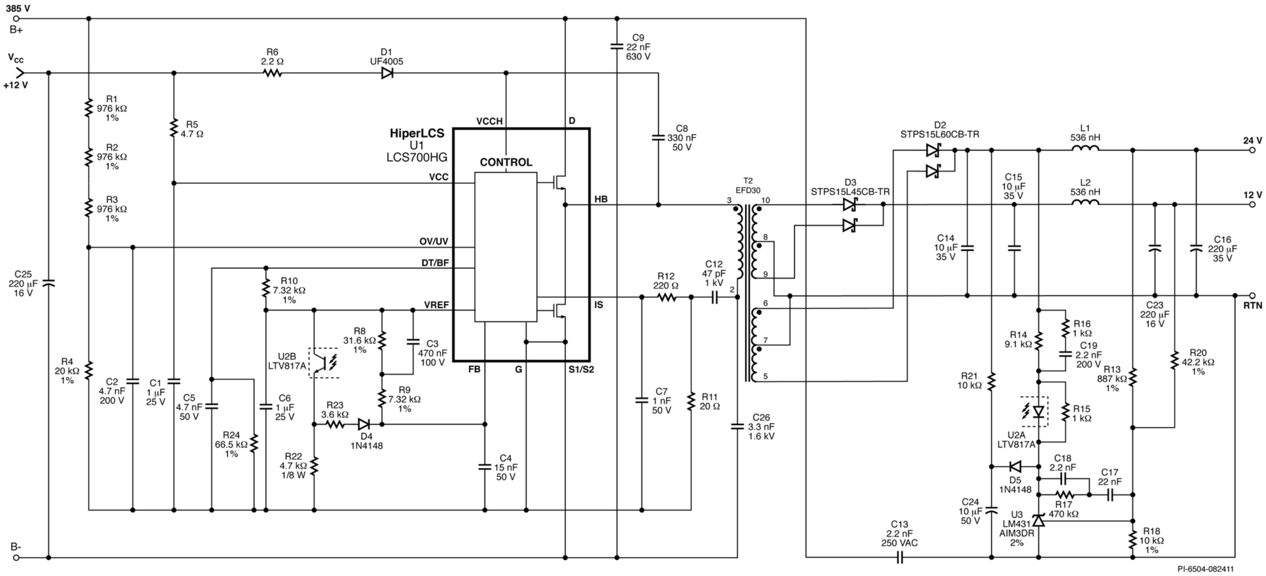

Figure 3 – Schematic.

5 Circuit Description

The schematic in Figure 3 depicts a 12 V / 24 V, 100 W LLC DC-DC converter implementing the LCS700HG device, intended for LCD TV applications. The circuit requires +12 V and +380 V input supplies to operate.

For proper operation, the board must be used with a bulk capacitor of at least 10 μF between the +380 V input and the input return placed directly across the terminals.

Do not apply greater than 15 V to the 12 V input or IC damage will result.

5.1 Primary

Integrated circuit U1 incorporates the control circuitry, drivers and output devices necessary for an LLC resonant half-bridge converter. The HB output pin of U1 drives output transformer T2 via a blocking/resonating capacitor (C26). This capacitor should be rated for the operating ripple current, and the voltage rating must be chosen to withstand the voltage present during fault conditions. Capacitor C26 fulfills these requirements.

Transformer T2 is designed for a leakage inductance of 100 μH. This, along with resonating capacitor C26, sets the primary series resonant frequency at ~280 kHz according to the equation:

$$f_R = \frac{1}{6.28\sqrt{L_L \times C_R}}$$

Where f_R is the series resonant frequency in hertz, L_L is the transformer leakage inductance in henries, and C_R is the value of the resonating capacitor (C26) in farads.

The transformer turns ratio was set by adjusting the primary turns, so that the operating frequency at nominal input voltage and full load, is close to but slightly less than the previously described resonant frequency. The secondary turns were chosen as a compromise between core and copper losses. AWG #42 Litz wire was used for the primary and secondary. This wire gauge provides good efficiency at ~270 kHz. The number of strands for each was chosen as a balance between fit and copper losses. The core material is Ferroxcube 3F3, which is well suited for high frequency operation. TDK PC95 would also work well. A 270 kHz operating frequency was found to be a good compromise between transformer size, output filter capacitance, and efficiency.

Components D1, R6, and C8 comprise the bootstrap circuit to supply the top side driver of U1. Components R5 and C1 are filtering and bypassing for the +12 V input. Voltage divider R1 to R4 sets the high-voltage turn-on and overvoltage thresholds of U1. The voltage divider values are chosen to set the LLC turn-on threshold at 360 VDC and the turn-off threshold at 285 VDC, with the nominal input overvoltage at 473 VDC.

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Capacitor C9 is a high frequency bypass capacitor for the +380 V input.

Capacitor C12 forms a current divider with C26, and is used to sample a portion of the primary current. Resistor R11 senses this current, and the resulting signal is filtered by R12 and C7. Capacitor C12 should be rated for the peak voltage present during fault conditions, and should use a stable, low loss dielectric such as film or NPO/COG ceramic. The values chosen set the 1 cycle (fast) current limit at ~3.2 A, and the 8 cycle (slow) current limit at ~1.8 A, according to the equation:

$$I_{CL} = \frac{0.5}{\left(\frac{C12}{C26 + C12}\right)(R11)}$$

I_{CL} is the 8-cycle current limit in Amperes, R11 is in Ohms, and C26 and C12 are the values of the resonating and current sampling capacitors in nano farad, respectively. For the one-cycle current limit, substitute 0.9 V for 0.5 V for the numerator in the above equation.

Resistor R12 and capacitor C7 filter primary current signal to the IS pin. Resistor R12 is set to the maximum allowable resistance of 220Ω. The value of C7 is set to 1 nF to avoid nuisance tripping due to noise, but not so high as to substantially affect the current limit set values as calculated above. These components should be placed directly at the IS pin for maximum effectiveness.

Resistor R10 sets the dead time at 320 ns. The FEEDBACK (FB) pin has an approximate characteristic of 2.6 kHz per μA into the FB pin. Current driven into the FB pin increases the operating frequency of U1, reducing the output voltage. The series combination of R8 and R9 sets the minimum operating frequency for U1. This value is generally set to somewhat lower than the frequency required for regulation with full load at output and minimum bulk capacitor voltage. Resistor R8 is bypassed by C3 to provide output soft start during start-up by initially allowing a higher current to flow into the FB pin when the feedback loop is open. This causes the switching frequency to start high and then decrease until the output voltage is in regulation. Resistor R9 is typically set at the same value as R10 so that the initial frequency at soft-start is equal to the maximum switching frequency as set by R10. Values of R9 below R10 cause a delay before switching commences.

Optocoupler U2 drives the feedback pin of IC U1. Capacitor C4 filters the FB pin. A 15 nF capacitor has been chosen for C4 in order to prevent asymmetry in the primary duty cycle due to noise coupled on the FB pin. Increasing C4 to a very high value typically results in instability.

Resistor R22 provides a load on the optocoupler, and speeds up the large signal transient response during burst mode. The recommended value is ~4.7 kΩ. Diode D4 prevents R22 from loading R8 when the optocoupler is cut off. Resistor R23 will improve the ESD and surge immunity of the PSU. It also improves burst mode output ripple voltage. Its maximum value must be such that the FB pin current is equal to the DT/BF pin current when the optocoupler is in saturation and the FB pin is at 2.0 V (please see PIXls HiperLCS spreadsheet). This is to ensure that if the HiperLCS does not exit start-up mode, because the feedback loop did not allow the switching frequency to drop below F_{STOP}, then it can regulate at light load by bursting at F_{MAX}.

During burst mode the power train can experience partial loss of ZVS (incomplete ZVS). If a large portion of the switching pulses lose ZVS, efficiency will be sacraficed. Sometimes the efficiency becomes noticeably lower at certain ranges of line and load. This can happen when the Burst Duty Cycle is high (15~30%) and most of the pulses have a significant loss of ZVS. This tends to get worse at high input voltage plus light load, e.g. 1% load, 420 VDC. ZVS loss can lead to device overheating and shutdown or damage. The condition is worsened by reducing dead-time (increasing F_{MAX}), and by increasing F_{START}, because higher operating frequency reduces transformer magnetizing current, which results in less stored energy in the transformer to charge and discharge the MOSFET output capacitance (C_{OSS}). In a real-world design, the PFC output voltage will not stay indefinitely at an anomalously high value, but instead will, in the case of a load-dump, return to nominal after a short time. This indicates that only maximum nominal PFC output voltages need to be considered when checking for burst mode ZVS loss.

5.2 Output Rectification

The outputs of transformer T2 are rectified and filtered by diodes D2 and D3 and capacitors C14 and C15. These capacitors are X5R dielectric, carefully chosen for output ripple current rating. Standard Z5U dielectric capacitors will **not** work in this application. Additional output filtering is provided by L1, L2, C16, and C23. Resistors R13, R20, and R18, along with the U3 reference voltage, set the output voltages of the supply. The voltage sensing resistors are set up such that the 12 V output dominates the overall regulation. Error amplifier U3 drives the feedback optocoupler U2 via R14. Components C17-19 and R14-17 determine the gain-phase characteristics of the converter.

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6 PCB Layout

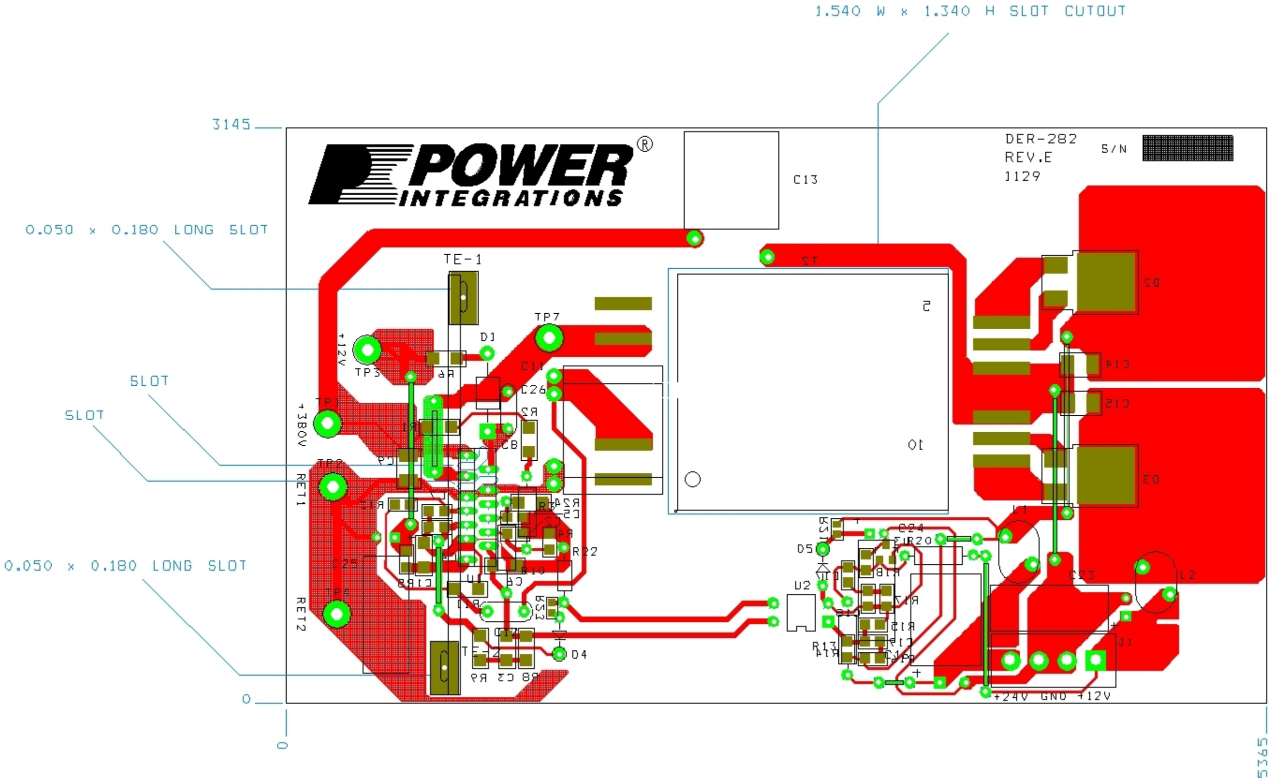

Figure 4 – Printed Circuit Layout

7 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	2	C1 C6	1 μF, 25 V, Ceramic, X7R, 1206	C3216X7R1E105K	TDK
2	1	C2	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX
3	1	C3	470 nF, 100 V, Ceramic, X7R, 1206	C3216X7R2A474K	TDK
4	1	C4	15 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H153K	Panasonic
5	1	C5	4.7 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H472K	Panasonic
6	1	C7	1 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H102K	Panasonic
7	1	C8	330 nF, 50 V, Ceramic, X7R	B37984M5334K000	Epcos
8	1	C9	22 nF, 630 V, Ceramic, X7R, 1210	GRM32QR72J223KW01L	Murata
9	1	C12	47 pF, 1000 V, Disc Ceramic	561R10TCCQ47	Vishay
10	1	C13	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
11	2	C14 C15	10 μF, 35 V, Ceramic, X5R, 1210	GMK325BJ106KN-T	Taiyo Yuden
12	1	C16	220 μF, 35 V, Electrolytic, Low ESR, 90 mΩ, (8 x 15)	ELXZ350ELL221MH15D	Nippon Chemi-Con
13	1	C17	22 nF, 200 V, Ceramic, X7R, 0805	08052C223KAT2A	AVX
14	1	C18	2.2 nF, 200 V, Ceramic, X7R, 0805	08052C222KAT2A	AVX
15	1	C19	2.2 nF, 50 V, Ceramic, X7R, 0805	ECJ-2VB1H222K	Panasonic
16	2	C23 C25	220 μF, 16 V, Electrolytic, Low ESR, 180 mΩ, (6.3 x 15)	ELXZ160ELL221MF15D	Nippon Chemi-Con
17	1	C24	10 μF, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG500ELL100ME11D	Nippon Chemi-Con
18	1	C26	3.3 nF, 1600 V, Film	B32652J1332J	Epcos
19	1	D1	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
20	1	D2	60 V, 7.5 A, Schottky, SMD, DPAK	STPS15L60CB-TR	ST
21	1	D3	45 V, 7.5 A, Dual Schottky, TO-252AA (D-PAK)	STPS15L45CB-TR	ST
22	2	D4 D5	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
23	1	ESIPCLIP M4 METAL1	Heat Sink Hardware, Edge Clip, 20.76 mm L x 8 mm W x 0.015 mm Thk	NP975864	Aavid Thermalloy
24	1	GREASE1	Thermal Grease, Silicone, 5 oz Tube	CT40-5	ITW Chemtronics
25	1	HS1	Heat Sink, Custom, Al, 3003, 0.62 Thk		Custom
26	1	J1	4 Position (1 x 4) header, 0.156 pitch, Vertical	26-48-1045	Molex
27	4	JP1 JP2 JP3 JP4	Wire Jumper, [high-temp. e.g. Teflon] Insulated, #22 AWG, 1 in	2855/1 WH005	AlphaWire
28	2	JP5 JP6	Wire Jumper, [high-temp. e.g. Teflon] Insulated, #22 AWG, 0.5 in	2855/1 WH005	AlphaWire
29	2	JP7 JP8	Wire Jumper, [high-temp. e.g. Teflon] Insulated, #22 AWG, 0.25 in	2855/1 WH005	AlphaWire
30	2	L1 L2	536 nH, Power Iron Toroid, 2 Pin, Output		
31	1	NUT1	Nut, Hex, Kep 4-40, S ZN Cr3 plating RoHS	4CKNTZR	Any RoHS Compliant Mfg.
32	2	R1 R2	976 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF9763V	Panasonic
33	1	R3	976 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-976K	Yageo
34	1	R4	20 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2002V	Panasonic
35	1	R5	4.7 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ4R7V	Panasonic
36	1	R6	2.2 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ2R2V	Panasonic
37	1	R8	31.6 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF3162V	Panasonic
38	1	R9	7.32 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF7321V	Panasonic
39	1	R10	7.32 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-7K32	Yageo
40	1	R11	20 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ200V	Panasonic
41	1	R12	220 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ221V	Panasonic
42	1	R13	887 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-887K	Yageo

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43	1	R14	9.1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ912V	Panasonic
44	2	R15 R16	1 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
45	1	R17	470 kΩ, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ474V	Panasonic
46	1	R18	10 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
47	1	R20	42.2 kΩ, 1%, 1/4 W, Metal Film	MFR-25FBF-42K2	Yageo
48	1	R21	10 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ103V	Panasonic
49	1	R22	4.7 kΩ, 5%, 1/8 W, Carbon Film	CFR-12JB-4K7	Yageo
50	1	R23	3.6 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ362V	Panasonic
51	1	R24	66.5 kΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF6652V	Panasonic
52	1	SCREW1	SCREW MACHINE PHIL 4-40 X 1/4 SS	PMSSS 440 0025 PH	Building Fasteners
53	1	T2	Custom Transformer, EFD30, Horz, 10 Pins (4 pri x 6 sec)		Power Integrations
54	1	TE1 TE2	Terminal, Eyelet, Tin Plated Brass, Zierick PN 190	190	Zierick
55	1	TP1	Test Point, YEL, THRU-HOLE MOUNT	5014	Keystone
56	2	TP2 TP4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
57	1	TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
58	1	TP7	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
59	1	U1	HiperLCS, ESIP16/13	LCS700HG	Power Integrations
60	1	U2	Optocoupler, 35 V, CTR 80-160%, 4-DIP	LTV-817A	Liteon
61	1	U3	IC, REG ZENER SHUNT ADJ SOT-23	LM431AIM3/NOPB	National Semi
62	1	WASHER1	WASHER FLAT #4 SS	FWSS 004	Building Fasteners

8 Transformer Specification

8.1 Electrical Diagram

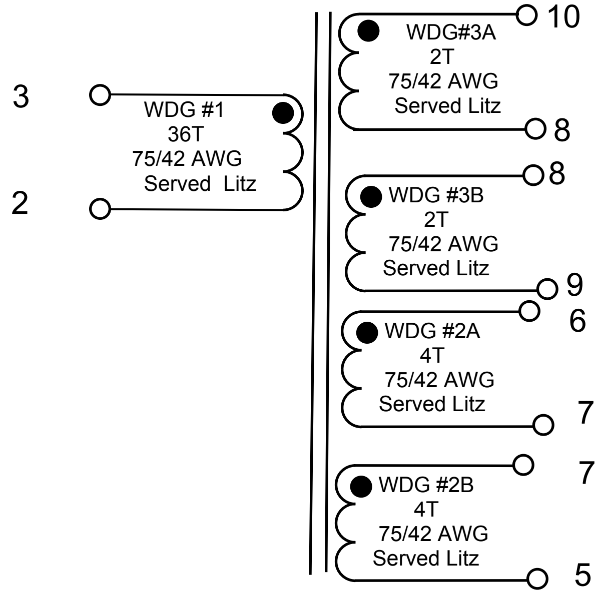

Figure 5 – Transformer Electrical Diagram.

8.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from 3-2 to 6-10	500 VAC
Primary Inductance	Pins 3-2, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	440 μH ±5%
Resonant Frequency	Pins 3-2, all other windings open	1400 kHz (Min)
Primary Leakage Inductance	Pins 3-2, with pins 5, 6, 7, 8, 9 and 10 shorted, measured at 100 kHz, 0.4 V_{RMS}	100 μH

8.3 Materials

Item	Description
[1]	Core Pair: EFD30 Ferroxcube 3F3 Material or equivalent
[2]	Bobbin: EFD30 Horizontal, 10 pin (4 Primary x 6 Secondary) Custom SMT Bobbin
[3]	Tape: Polyester Web: 3M #44 or equivalent, 3.0 mm wide.
[4]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 12.2 mm wide.
[5]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 5 mm wide.
[6]	Magnet wire: 75/#42 Single Coated Served Litz wire.
[7]	Transformer Varnish Dolph BC-359 or equivalent.

Note: The transformer may need to be redesigned for some applications to meet safety requirements.

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8.4 Transformer Build Diagram

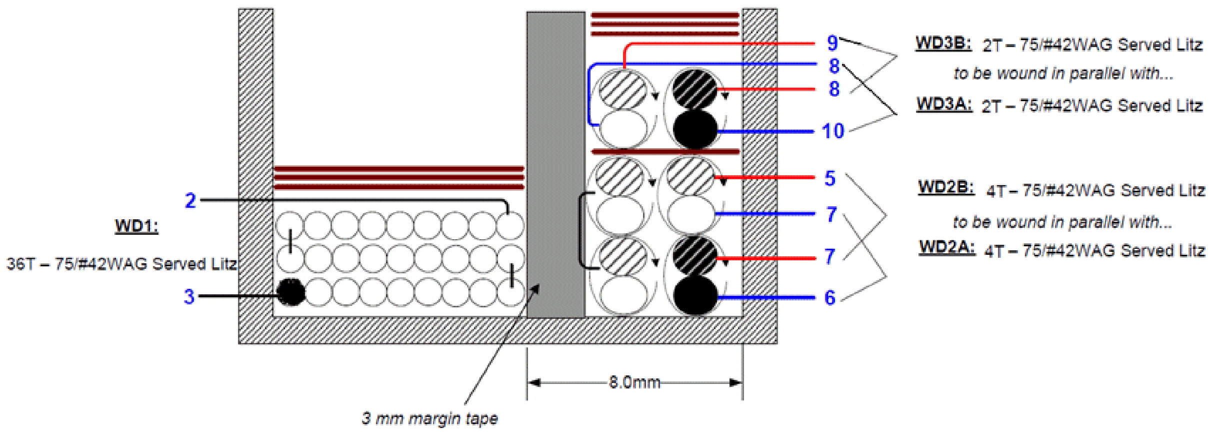

Figure 6 – Transformer Build Diagram.

8.5 Bobbin – Numbering Convention

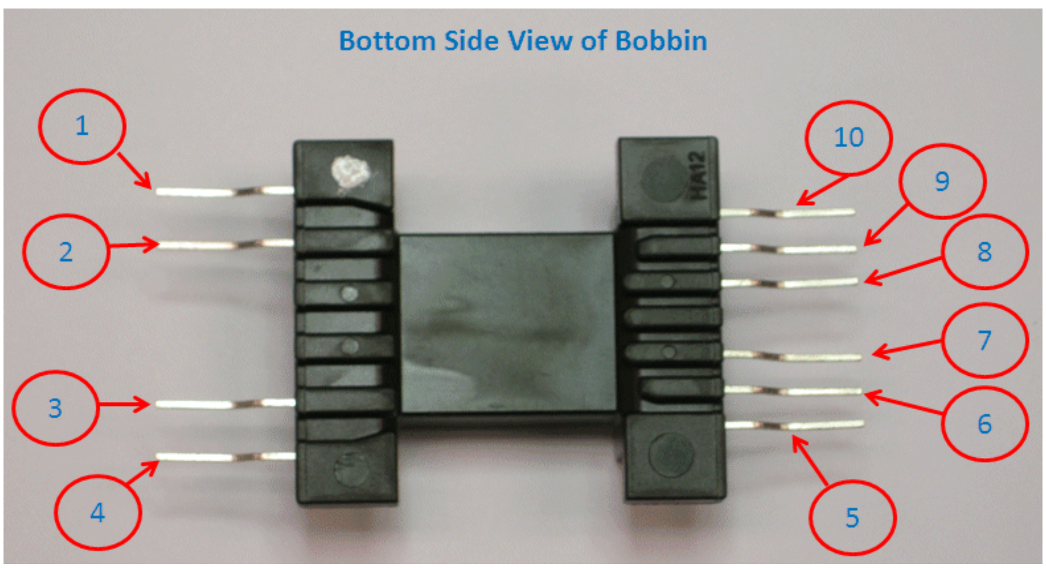

Figure 7 – Bobbin Pin Convention.

8.6 Transformer Construction

Winding Preparation	To allow for proper fitting of core halves, use a fine course file to remove approximately 0.5 mm of bobbin material from the short flanges on both the primary and secondary sides. Place margin tape [3] on the right side of bobbin as shown, with leftmost edge of tape 8 mm away from bobbin right-hand side.
WD1 (Primary)	Starting in position shown, wind 36 turns of Litz wire [6] on left-hand side of bobbin in ~ 3 layers. Use 1 layer of tape [4] to secure winding.
Secondary Wire Preparation	Prepare 2 strands of Litz wire item [6] 15” length, tin ends twist these 2 strands together ~65 twists evenly along length leaving 1” free at each end. One end of this cable will be 6 and 7, the other 7 and 5.
WDG2A and WDG2B (Secondary)	Starting with 6 and 7 as shown, wind 4 turns in the section between margin tape and right-hand side of bobbin, and exit with 7 and 5 as shown.
Insulation	Secure winding with one turn of tape [5].
Secondary Wire Preparation	Prepare 2 strands of Litz wire [6] 7.5” in length, tin ends. Twist strands together ~30 twists evenly along length leaving 1” free at each end. One end of this cable will be 10 and 8, the other 8 and 9.
WDG3A and WDG3B (Secondary)	Starting with 10 and 8 as shown, wind 2 turns in the section between margin tape and right-hand side of bobbin, and exit with 8 and 9 as shown.
Insulation	Apply 1 layers of tape item [5] to secure windings.
Finish	Grind center leg of one core half to achieve 440 μH ±5% inductance between pins 2 and 3. Assemble core halves with the core with ground center leg on the primary side of the bobbin. Dip varnish (item [7]).

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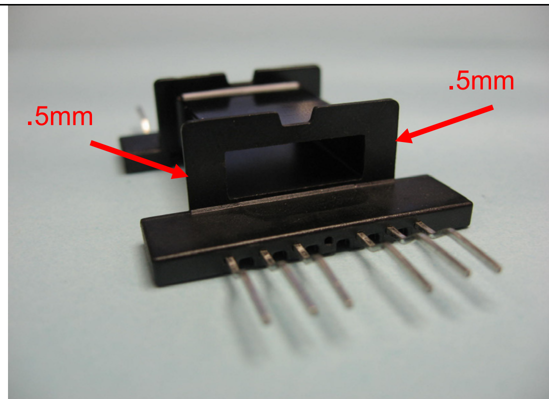
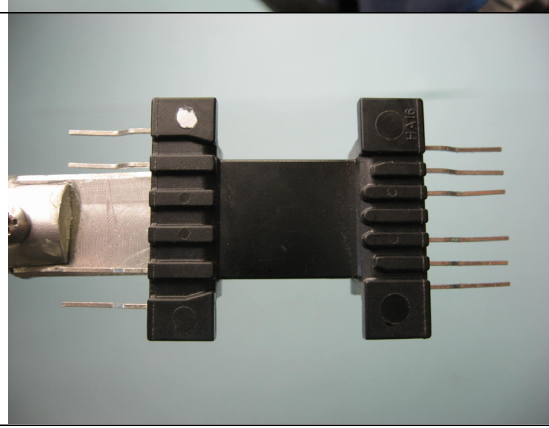
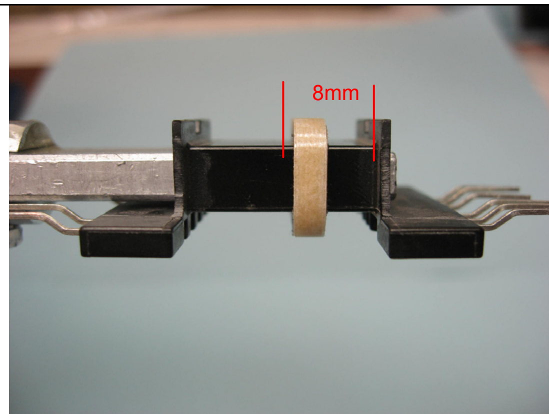
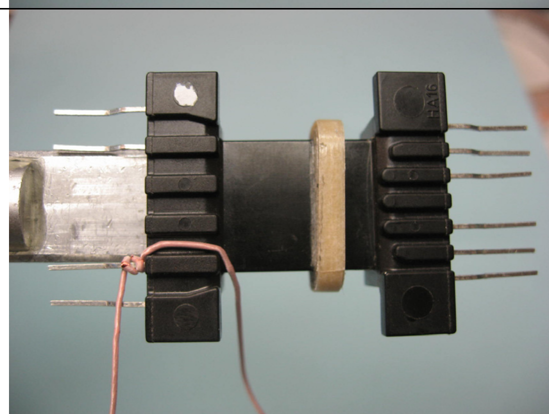
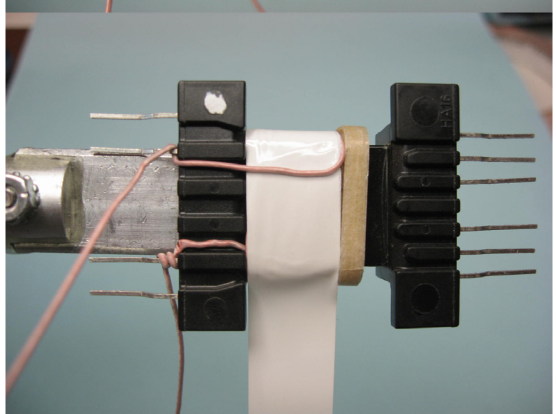
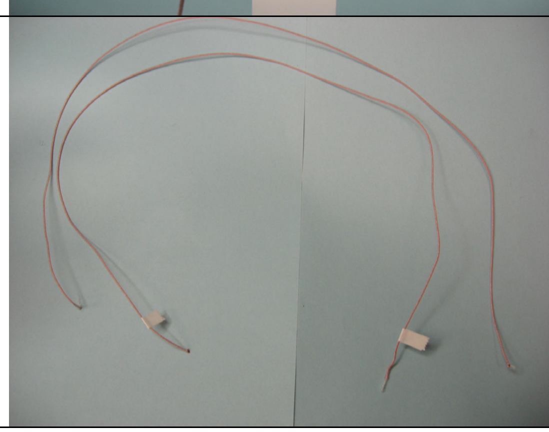
8.7 Winding Illustrations

Bobbin Preparation		To allow for proper fitting of core halves, use a fine course file to remove approximately .5 mm of bobbin material from the short flanges on both the primary and secondary sides.
Barrier Tape		Place the bobbin item [2] on the mandrel with pin 1 on the left side. Measure 8 mm from secondary flange and wind 20 turns of 3 mm barrier tape [3]. Tape height should be flush with the height of the bobbin flanges.

		
WD1 (Primary)		Starting on pin 3, wind 36 turns of served Litz wire [6] in 3 layers, and finish on pin 2. Secure winding with three turns of tape [4].
WD2 Preparation		Cut two strands of served Litz wire [6] to lengths of 15 inches each. On one strand of wire, mark the ends with tape or some other type of marking material. Twist both strands together with ~65 twists. Leave about an inch free at each end.

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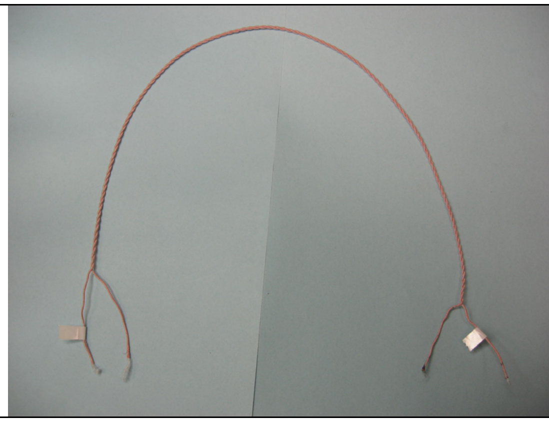
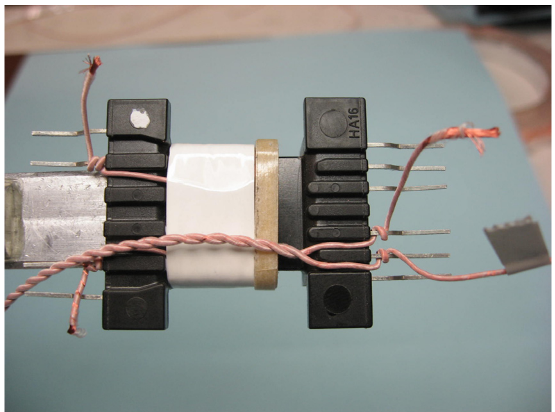
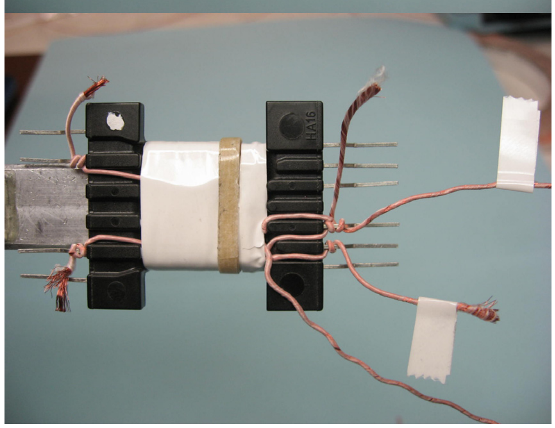
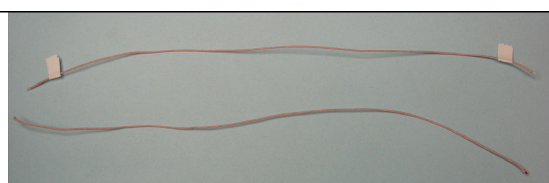
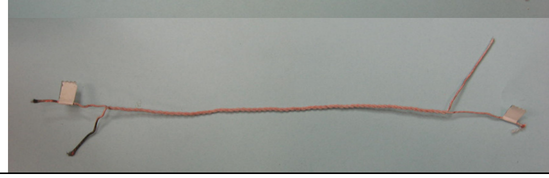
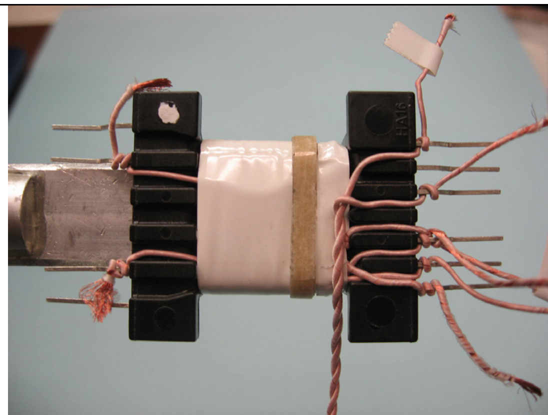
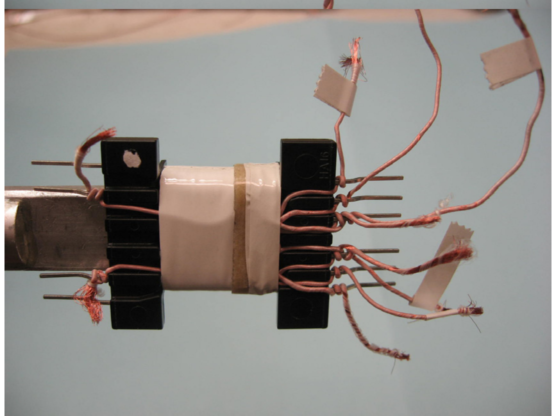
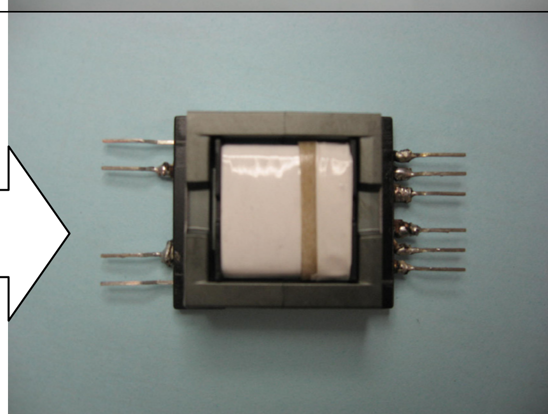
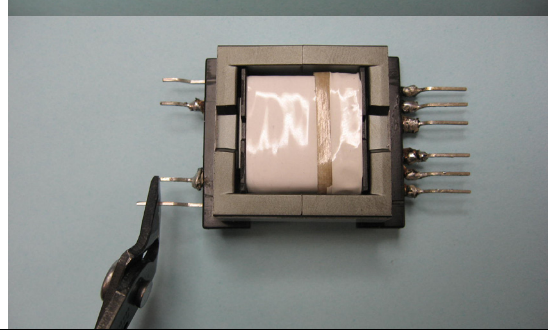
		
WD2A and WD2B (Secondary)	 	Using the served Litz assembly prepared in the previous step, start with the marked end on pin 6 and the unmarked end on pin 7 and wind 4 turns. Finish with the marked end on pin 7 and the unmarked end on pin 5. Secure winding with one turn of tape [5].
WD3 Preparation	 	Cut two strands of served Litz wire [6] to lengths of 7 inches each. On one strand of wire, mark the ends with tape or some other type of marking material. Twist both strands together with ~30 twists. Leave about an inch free at each end.

WD3A and WD3B (Secondary)	 	Using the served Litz assembly prepared in the previous step, start with the marked end on pin 10 and the unmarked end on pin 8 and wind 2 turns. Finish with the marked end on pin 8 and the unmarked end on pin 9. Secure winding with three turns of tape [5].
Finish Insert core with ground center leg on left side of the bobbin	 	Solder all wire terminations. Grind center leg of one core half [1] for an inductance of 440 μH ±5% between pins 2 and 3. Assemble and secure core halves, with the ground core on the primary side (left side in the picture). Trim 3.5 mm from each bobbin pin.

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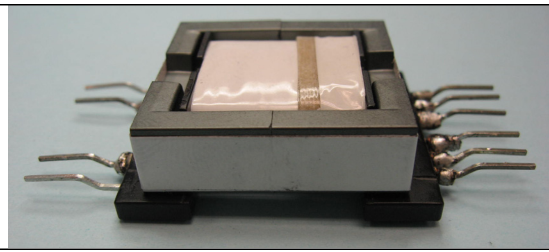
Finish (con't)		Dip varnish [7].

9 Output Inductor Specification

Inductors L1 and L2 are each 4 turns of #22 AWG magnet wire on a Micrometals T30-26 powdered iron toroid.

9.1 Electrical Specifications

Inductance	Pins FL1–FL2, all other windings open, measured at 100 kHz, 0.4 V_{RMS}	536 nH, ±15%

9.2 Material List

Item	Description
[1]	Powdered Iron Toroidal Core: Micrometals T30-26
[2]	Magnet wire: #22 AWG Solderable Double Coated

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10 LLC Resonant Converter Design Spreadsheet

HiperLCS_041311; Rev.1.0; Copyright Power Integrations 2011	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_041311_Rev1-0.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					
VBULK_NOM			380	V	Nominal LLC input voltage
Vbrownout			280	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of VBULK_NOM. Set to 65% for max holdup time
Vbrownin			353	V	Startup threshold on bulk capacitor
VOV_shut			465	V	OV protection on bulk voltage
VOV_restart			448	V	Restart voltage after OV protection.
CBULK			69	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbulkmin to change bulk cap value
tHOLDUP			21.8	ms	Bulk capacitor hold up time
Enter LLC (secondary) outputs					**The spreadsheet assumes AC stacking of the secondaries**
VO1	12.00		12.0	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	2.32		2.3	A	Main output maximum current
VD1	0.60		0.60	V	Forward voltage of diode in Main output
PO1			28	W	Output Power from first LLC output
VO2	24.00		24.0	V	Second Output Voltage
IO2	3.00		3.0	A	Second output current
VD2	0.60		0.60	V	Forward voltage of diode used in second output
PO2			72.00	W	Output Power from second LLC output
P_LLC			100	W	Specified LLC output power
LCS Device selection					
Device	**Auto**		**LCS700**		LCS Device
RDSON (MAX)			2.78	ohms	RDSON (max) of selected device
Coss			125	pF	Equivalent Coss of selected device
Cpri			40	pF	Stray Capacitance at transformer primary
PCOND_LOSS			1.3	W	Conduction loss at nominal line and full load
TMAX_HS			90	deg C	Maximum heatsink temperature
Theta J-HS			10.1	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature			103	deg C	Expectd Junction temperature
Ta max			50	deg C	Expected max ambient temperature
Theta HS-A			31	deg C/W	Required thermal resistance heatsink to ambient
LLC Resonant Parameter and Transformer Calculations (generates red curve)					
Po			103	W	Output from LLC converter including diode loss
Vo			12.60	V	Main Output at transformer windings (includes diode drop)
f_target			250	kHz	Desired full load switching frequency of PFC and LLC. 66 kHz to 300 kHz, recommended 250 kHz
Lpar			340	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)
Lpri	440.00		440	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for loss of ZVS at 80% of Vnom
Lres	100.00		100.0	uH	Series inductance or primary leakage inductance of integrated transformer; if left blank auto-calculation is for K=4
Kratio			3.4		Ratio of Lpar to Lres. Maintain value of K such that 2.1 < K < 11. Preferred Lres is such that K<7.

Cres	3.30		3.3	nF	Series resonant capacitor. Red background cells produce red graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec			1.358	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
m			50	%	Leakage distribution factor (primary to secondary). 99% signifies most of the leakage is in primary side
n_eq			15.82		Turns ratio of LLC equivalent circuit ideal transformer
Npri	36.0		36.0		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target
Nsec	2.0		2.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain BAC<=2000 Gauss
f_predicted			247	kHz	Expected frequency at nominal input voltage and full load; Heavily influenced by n_Ratio and primary turns
f_res			277	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout			192	kHz	Switching frequency at VBULK_MIN, full load
f_par			132	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion			179	kHz	Min frequency, at Vbrownout and full load. Set HiperLCS minimum frequency to this value. Operation below this frequency results inoperation in gain inversion region
Vinversion			252	V	Minimum input voltage of LLC power train before low freq gain inversion point. Optimum value is equal Vbrownout
RMS CURRENTS AND VOLTAGES					
IRMS_LLC_Primary			0.68	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and fnominal_actual
Winding 1 (Lower secondary Voltage) RMS current			4.1	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current			1.1	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			2.3	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current			1.4	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms			133	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage
Virtual Transformer Trial - (generates blue curve)					
New primary turns			36.0		Trial transformer primary turns; default value is from resonant section
New secondary turns			2.0		Trial transformer secondary turns; default value is from resonant section
New Lpri			440	uH	Trial transformer open circuit inductance; default value is from resonant section
New Cres	3.30		3.3	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res = f_target
New estimated Lres			100.0	uH	Trial transformer estimated Lres
New estimated Lpar			340	uH	Estimated value of Lpar for trial transformer
New estimated Lsec			1.358	uH	Estimated value of secondary leakahe inductance
New Kratio			3.4		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio			15.82		Estimated effective transformer turns ratio

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V powertrain inversion new			252	V	Voltage on Bulk Capacitor below which ZVS is lost
f_res_trial			277	kHz	New Series resonant frequency
f_predicted_trial			247	kHz	New nominal operating frequency
IRMS_LLC_Primary			0.68	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current			4.1	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape; Output 2 winding is AC stacked on top of Output 1 winding
Lower Secondary Voltage Capacitor RMS current			1.1	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			2.3	A	RMS current through Output 2 winding
Higher Secondary Voltage Capacitor RMS current			1.4	A	Higher Secondary Voltage Capacitor RMS current
TRANSFORMER CORE CALCULATIONS (calculates from resonant parameter section)					
Transformer Core	**Auto**		**EFD30**		**Transformer Core**
Ae			0.7	cm^2	Enter transformer core cross-sectional area
Ve			4.7	cm^3	Enter the volume of core
Aw			52.3	mm^2	Area of window
Bw			20.1	mm	Total Width of Bobbin
Loss density			200.0	mW/cm^3	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m^3)
MLT			3.7	cm	Mean length per turn
N_CHAMBERS			2.0		Number of Bobbin chambers
W_SEP			3.0	mm	Winding separator distance (will result in loss of winding area)
Ploss			0.9	W	Estimated core loss
Bpkfmin			119	mT	First Quadrant peak flux density at minimum frequency.
BAC			185	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)
PRIMARY WINDING					
Npri			36.0		Number of primary turns; determined in LLC resonant section
Primary gauge	42		42	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge			0.060	mm	Equivalent diameter of wire in metric units
Primary litz strands	75		75		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor			50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P			22	mm^2	Winding window area for primary
Fill Factor			57%	%	% Fill factor for primary winding (typical max fill is 60%)
Resistivity_25 C_Primary			79.06	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C			105.25	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C			141.03	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current			0.68	A	Measured RMS current through the primary winding
ACR_Trf_Primary			225.65	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss			0.11	W	Total primary winding copper loss at 85 C
Secondary winding 1 (Lower secondary voltage OR Single output)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			12.00	V	Output Voltage (assumes AC stacked windings)
Sec 1 Turns			2.00		Secondary winding turns (each phase)

Sec 1 RMS current (total, AC+DC)			4.1	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape; Output 2 winding is AC stacked on top of Output 1 winding
Winding current (DC component)			2.66	A	DC component of winding current
Winding current (AC RMS component)			3.17	A	AC component of winding current
Sec 1 Wire gauge	42		42	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge			0.060	mm	Equivalent diameter of wire in metric units
Sec 1 litz strands	75		75		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1			79.06	m-ohm/m	Resistivity in milli-ohms per meter
DCR_25C_Sec1			5.85	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1			7.84	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.44	W	Estimated Power loss due to DC resistance (both secondary phases)
ACR_Sec1			12.54	m-ohm	Measured AC resistance per phase(at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature . Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1			0.25	W	Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses			0.70	W	Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current			1.1	A	Output capacitor RMS current
Co1	10.00		10.0	uF	Secondary 1 output capacitor
Capacitor ripple voltage			1.2	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Secondary winding 2 (Higher secondary voltage)					**Note - Power loss calculations are for each winding half of secondary**
Output Voltage			24.00	V	Output Voltage (assumes AC stacked windings)
Sec 2 Turns			2.00		Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)			2.3	A	RMS current through Output 2 winding
Winding current (DC component)			1.5	A	DC component of winding current
Winding current (AC RMS component)			1.8	A	AC component of winding current
Sec 2 Wire gauge	42		42	AWG	Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge			0.060	mm	Equivalent diameter of wire in metric units
Sec 2 litz strands	75		75		Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec2			79.06	m-ohm/m	Resistivity in milli-ohms per meter
Transformer Secondary MLT			3.70	cm	Mean length per turn
DCR_25C_Sec2			5.85	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2			7.84	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.14	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2			12.54	m-ohm	Measured AC resistance per phase(at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature . Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2			0.08	W	Estimated AC copper loss (both secondary halves)
Total winding 2			0.22	W	Total (AC + DC) winding copper loss for both

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Copper Losses					secondary halves
Capacitor RMS current			1.4	A	Output capacitor RMS current
Co2	10.00		10.0	uF	Secondary 2 output capacitor
Capacitor ripple voltage			0.8	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Transformer Loss Calculations					**Does not include fringing flux loss from gap**
Primary copper loss (from Primary section)			0.11	W	Total primary winding copper loss at 85 C
Secondary copper Loss			0.92	W	Total copper loss in secondary winding
Transformer total copper loss			1.02	W	Total copper loss in transformer (primary + secondary)
AW_S			22.25	mm^2	Area of window for secondary winding
Secondary Fill Factor			13%	%	% Fill factor for secondary windings; typical max fill is 60% for served and 75% for unserved Litz
Signal pins resistor values					
Dead Time			320	ns	Dead time
Burst Mode	**Auto**		**2**		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max			797	kHz	Max internal clock frequency, dependent on dead-time setting
f_burst_start			299	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period
f_burst_stop			349	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor			7.21	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor			65	k-ohms	Resistor from DT/BF pin to G pin
Rstart	7.32		7.32	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup
Start up delay			0.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin			31.8	k-ohms	Resistor from VREF pin to FB pin, to set min operating frquency; This resistor plus Rstart determine f_MIN
C_softstart	1		1.0	uF	Softstart capacitor. Recommended values are between 0.1 uF and 10 uF
Ropto			3.8	k-ohms	Resistor in series with opto emitter
OV/UV pin lower resistor	20.00		20.0	k-ohm	Lower resistor in OV/UV pin divider
OV/UV pin upper resistor			2.92	M-ohm	Total upper resistance in OV/UV pin divider
LLC capacitive divider current sense circuit					
slow current limit			1.91	A	8-cycle current limit - check postivie half-cycles during brownout and startup
fast current limit			3.44	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor			47	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor	20		18.6	ohms	LLC current sense resistor, senses current in sense capacitor
IS pin current limit resistor			220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor			1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency			724	kHz	This pole attenuates IS pin signal
LOSS BUDGET					
LCS device Conduction loss			1.3	W	Conduction loss at nominal line and full load

Output diode Loss			1.4	W	Estimated diode losses
Transformer estimated total copper loss			1.02	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss			0.9	W	Estimated core loss
Total transformer losses			2.0	W	Total transformer losses
Total estimated losses			4.7	W	Total losses in LLC stage
Estimated Efficiency			96%	%	Estimated efficiency
PIN			104	W	LLC input power
SECONDARY TURNS AND VOLTAGE CENTERING CALCULATOR					**This is to help you choose the secondary turns - Outputs not connected to any other part of spreadsheet**
V1			12.00	V	Target regulated output voltage Vo1. Change to see effect on slave output
V1d1			0.60	V	Diode drop voltage for Vo1
N1			2.00		Total number of turns for Vo1
V1_Actaul			12.00	V	Expected output
V2			24.00	V	Target output voltage Vo2
V2d2			0.60	V	Diode drop voltage for Vo2
N2			4.00		Total number of turns for Vo2
V2_Actual			24.60	V	Expected output voltage
Separate Series Inductor (For non-integrated transformer only)					**Not applicable if using integrated magnetics - not connected to any other part of spreadsheet**
Lsep			100.00	uH	Desired inductance of separate inductor
Ae_Ind			0.53	cm^2	Inductor core cross-sectional area
Inductor turns			13		Number of primary turns
BP_fnom			1501	Gauss	AC flux for core loss calculations (at f_predicted and full load)
Expected peak primary current			1.9	A	Expected peak primary current
BP_fmin			2802	Gauss	Peak flux density, calculated at minimum frequency fmin
Inductor gauge			44	AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor Metric Wire gauge			0.050	mm	Equivalent diameter of wire in metric units
Inductor litz strands			125.00		Number of strands used in Litz wire
Inductor parallel wires			1		Number of parallel individual wires to make up Litz wire
Resistivity_25 C_Sep_Ind			75.4	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT			7.00	cm	Mean length per turn
Inductor DCR 25 C			68.6	m-ohm	Estimated resistance at 25 C (for reference)
Inductor DCR 100 C			92.0	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
ACR_Sep_Inductor			147.1	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss			0.07	W	Total primary winding copper loss at 85 C

Note: The spreadsheet calculation of secondary turns assumes AC stacking of output windings. AC stacking has not been used for transformer construction in this design.

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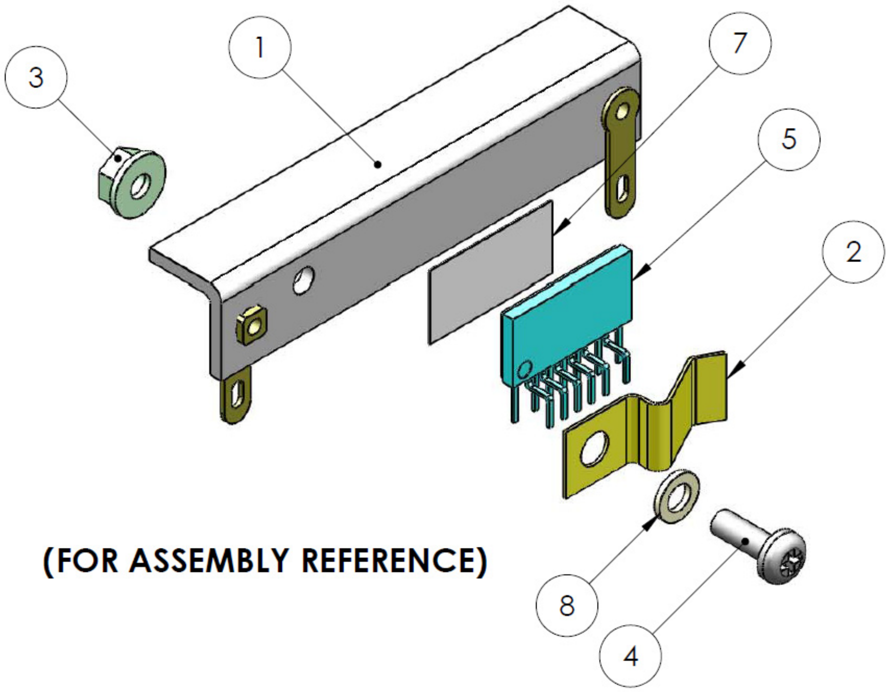
11 Heat Sink Assembly



Item#	Item Description
1	Heat Sink
2	Metal Clip
3	Kep Nut
4	Screw
5	HiperLCS IC
6	N.A.
7	Thermal Grease
8	Flat Washer

Figure 8 – Before Assembly.

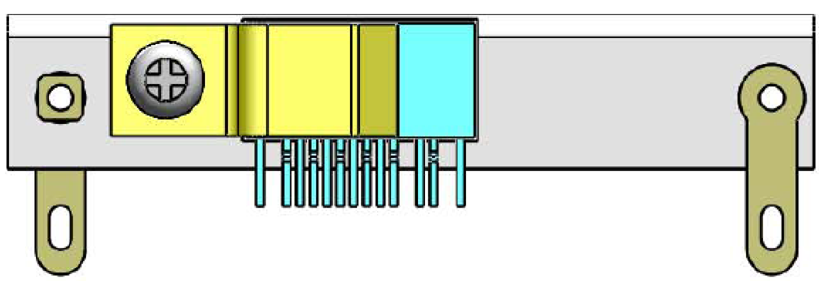


Figure 9 – After Assembly.

12 Performance Data

12.1 *Efficiency – 100%, 50%, 20% and 10% Load*

12.1.1 Efficiency Data

P_{IN}	V_{OUT} (24 V)	I_{OUT} (24 V)	V_{OUT} (12 V)	I_{OUT} (12 V)	P_{OUT}	Efficiency (%)
107.05	24.27	2.999	11.99	2.327	100.686	94.06
53.97	24.24	1.503	11.99	1.164	50.389	93.36
22.365	24.22	0.6027	11.99	0.4608	20.122	89.97
11.985	24.22	0.3027	11.99	0.2266	10.048	83.84

12.2 *Output Cross Regulation*

To obtain the data shown below, one output was adjusted to maximum load (3 A), while the other was varied between zero load and the maximum load consistent with a maximum total output power of 100 W.

12.2.1 Cross Regulation Data

Cross Regulation with 12 V at 3 A				Cross Regulation with 24 V at 3 A			
V_{OUT} (24 V)	I_{OUT} (24 V)	V_{OUT} (12 V)	I_{OUT} (12 V)	V_{OUT} (24 V)	I_{OUT} (24 V)	V_{OUT} (12 V)	I_O (12 V)
25.31	0.0105	11.94	3	22.84	3	12.07	0.012
25.25	0.0206	11.94	3	23.21	3	12.05	0.02
25.21	0.0318	11.94	3	23.28	3	12.05	0.0314
25.16	0.0514	11.95	3	23.35	3	12.04	0.0507
25.08	0.1024	11.95	3	23.46	3	12.04	0.1008
24.98	0.2506	11.95	3	23.64	3	12.03	0.251
24.9	0.5014	11.96	3	23.79	3	12.02	0.4997
24.78	0.9992	11.96	3	23.96	3	12.01	1.0016
24.6	2	11.97	3	24.21	3	11.99	2.001
24.49	2.645	11.98	3	24.29	3	11.99	2.324

12.3 *Start and Shutdown Bulk Voltage*

With +12 VDC applied to the VCC input, output start up voltage was 357.4 VDC, output shutdown occurred at 283.9 VDC.

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13 Waveforms

13.1 Half Bridge Voltage and Current, Normal Operation

13.1.1 Measured at 380 VDC input

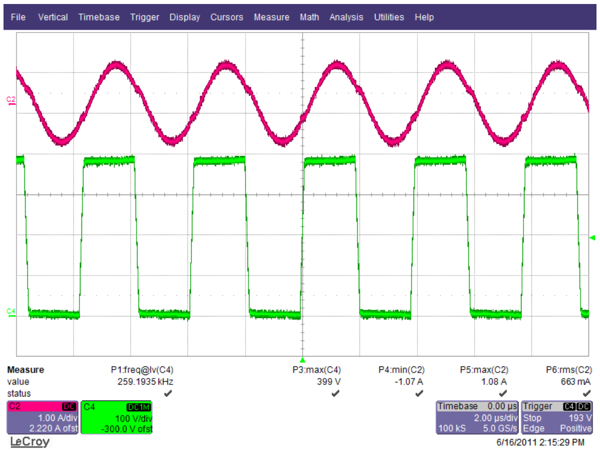

Figure 10 – Primary V-I, Full Load.
Upper: Primary Current, 1 A / div.
Lower: HB to Primary Ground Voltage, 100 V, 2 µs / div.

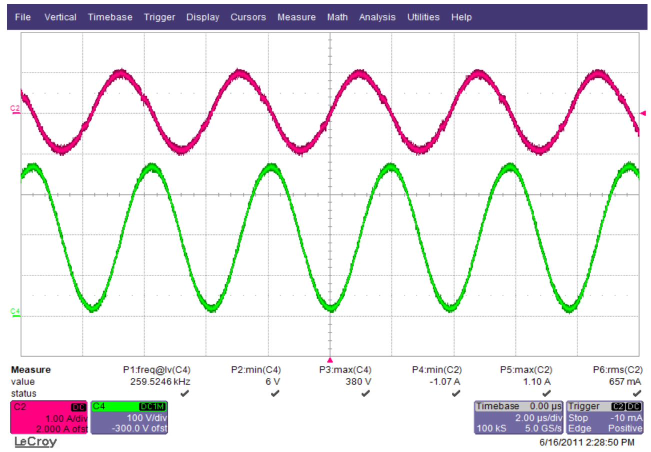

Figure 11 – Primary V-I, Full Load.
Upper: Primary Current, 1 A / div.
Lower: Resonating Capacitor (C11) Voltage, 100 V, 2 µs / div.

13.2 Output Voltage Start-up Profile

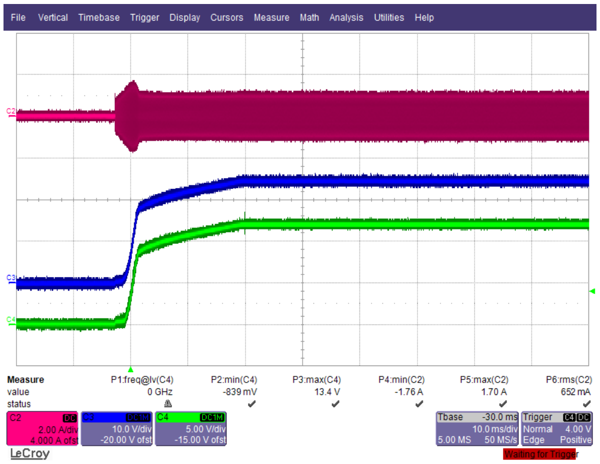

Figure 12 – Full Load Start-up.
Upper: Primary Current, 1 A / div.
Middle: 24 V_{OUT}, 10 V / div.,
Lower: 12 V_{OUT}, 5 V, 10 ms/ div.

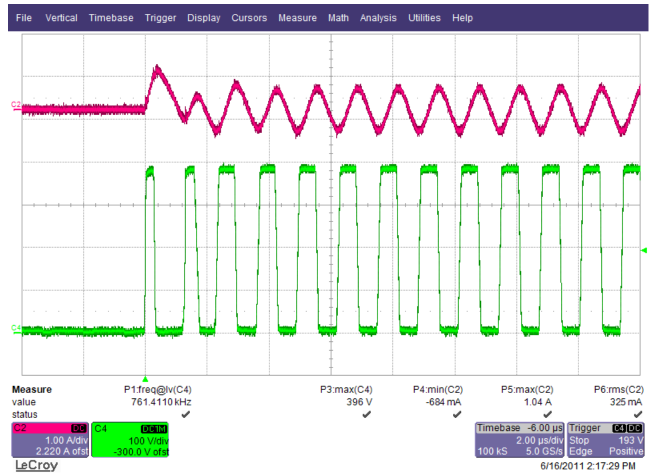

Figure 13 – Full Load Start-up.
Upper: Primary Current, 1 A / div.
Lower: HB to Primary Ground Voltage,
100 V, 2 µs / div.

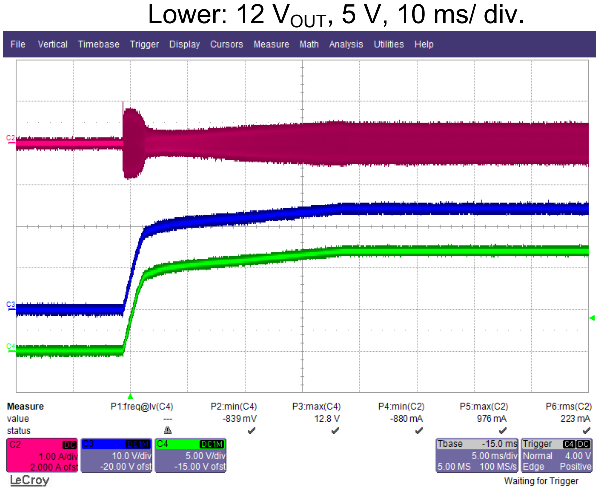

Figure 14 – Output Voltages at Start-up, No-Load.
Upper: Primary Current, 1 A / div.
Middle: 24 V_{OUT}, 10 V / div.,
Lower: 12 V_{OUT}, 5 V, 5 ms / div.

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13.3 Load Transient Response (5% to 100% Load Step at 380 VDC Input)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

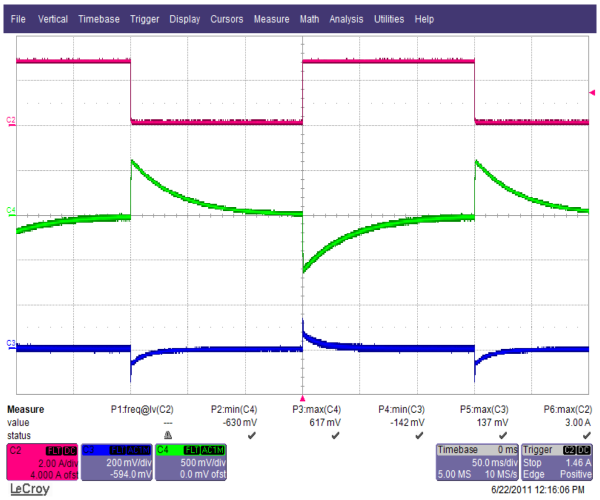

Figure 15 – 5%-100% Load Transient on 24 V_{OUT} 10% Load on 12 V_{OUT}.
Upper: 24 V_{OUT} Load Current, 2 A / div.
Middle: 24 V_{OUT} AC Coupled, 500 mV / div.
Lower: 12 V_{OUT} AC Coupled, 200 mV / div, 50 mS / div.

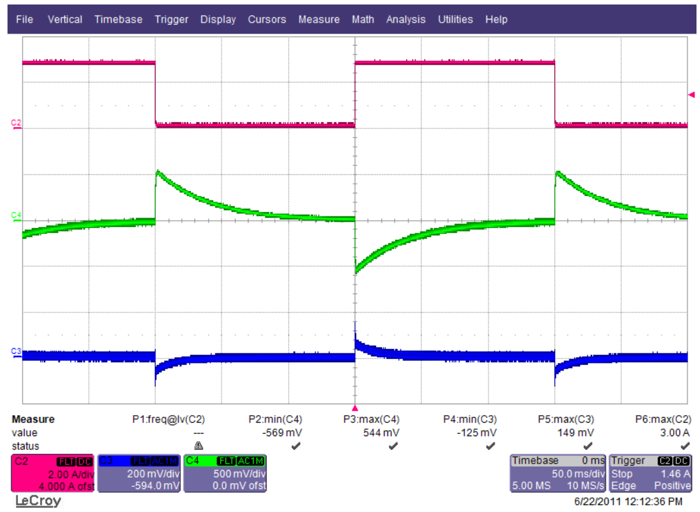

Figure 16 – 5%-100% Load Transient on 24 V_{OUT} 100% Load on 12 V_{OUT}.
Upper: 24 V_{OUT} Load Current, 2 A / div.
Middle: 24 V_{OUT} AC Coupled, 500 mV / div.
Lower: 12 V_{OUT} AC Coupled, 200 mV / div, 50 mS / div.

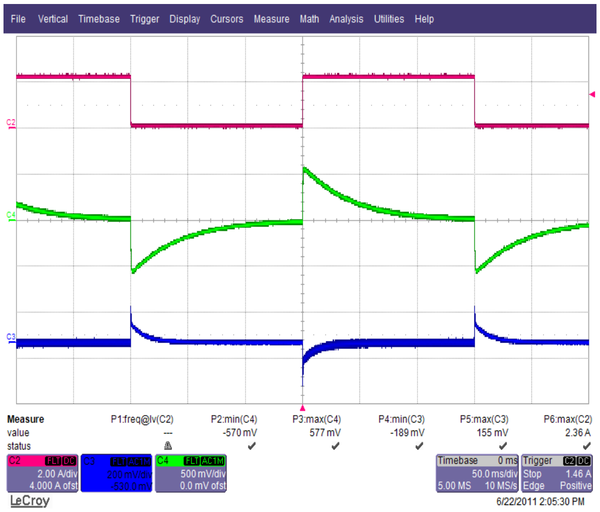

Figure 17 – 5%-100% Load Transient on 12 V_{OUT}, 10% Load on 24 V_{OUT}.
Upper: 12 V_{OUT} Load Current, 2 A / div.
Middle: 24 V_{OUT} AC Coupled, 500 mV / div.
Lower: 12 V_{OUT} AC Coupled, 200 mV / div, 50 mS / div.

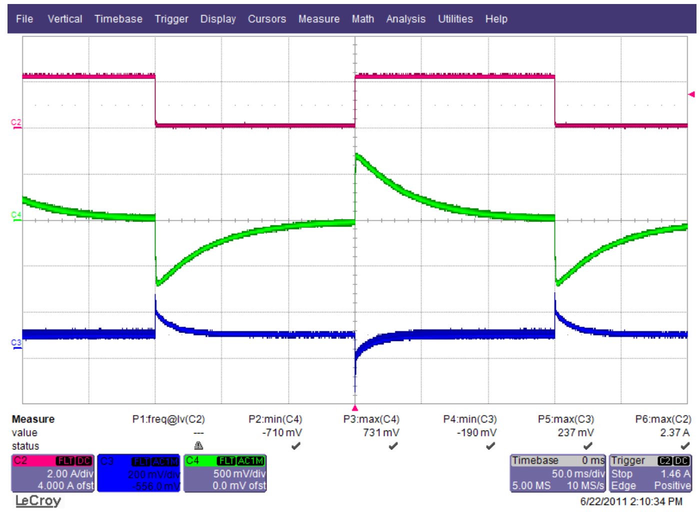

Figure 18 – 5%-100% Load Transient on 12 V_{OUT}, 100% Load on 24 V_{OUT}.
Upper: 12 V_{OUT} Load Current, 2 A / div.
Middle: 24 V_{OUT} AC Coupled, 500 mV / div.
Lower: 12 V_{OUT} AC Coupled, 200 mV / div, 50 mS / div.

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13.4 Output Brown-out

Figures 12 and 13 taken by switching off input voltage supply and triggering oscilloscope on falling edge of 24 V output.

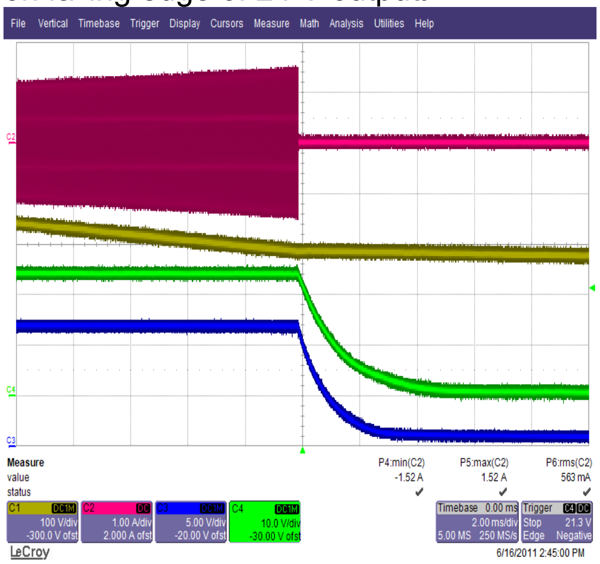

Figure 19 – Output Brown-out.
Upper: Primary Current, 1 A / div.
2nd Trace: Primary Bus Voltage, 100 V / div.
3rd Trace: 24 V_{OUT}, 10 V / div.
4th Trace: 12 V_{OUT}, 5 V, 2 ms / div.

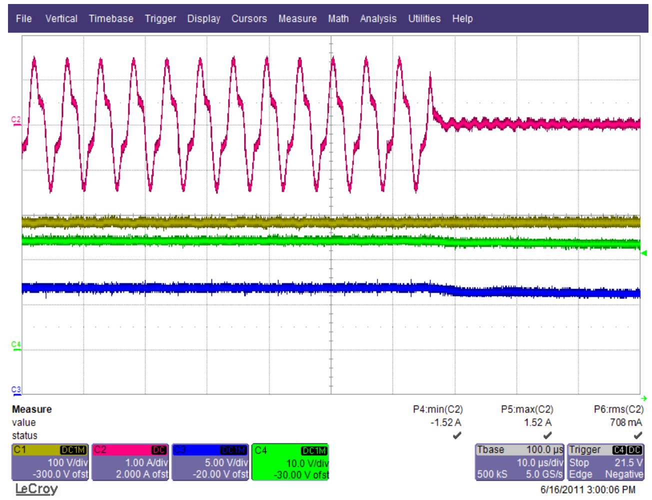

Figure 20 – Output Brown-out.
Upper: Primary Current, 1 A / div.
2nd Trace: Primary Bus Voltage, 100 V / div.
3rd Trace: 24 V_{OUT}, 10 V / div.
4th Trace: 12 V_{OUT}, 5 V, 10 μs / div.

13.5 *Output Diode Peak Reverse Voltage*

The following waveforms were measured at full load and 380 VDC input.

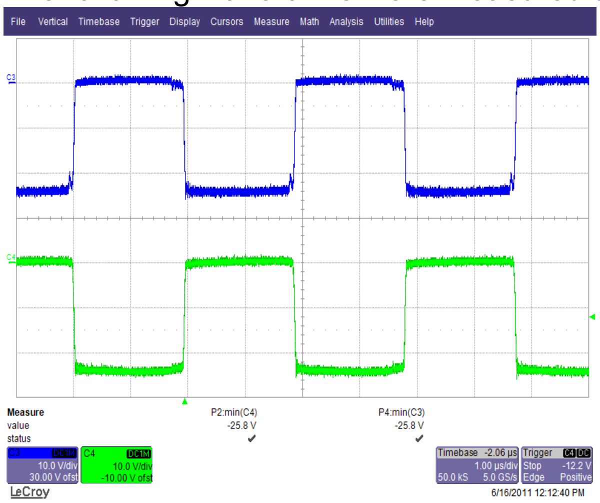

Figure 21 – 12 V Output Diodes (D3 Dual Package Common Cathode), 380 VDC Input, 10 V, 1 µs / div.

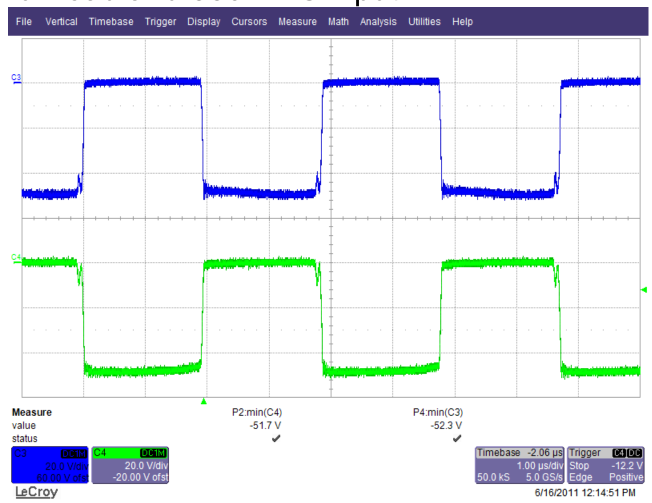

Figure 22 – 24 V Output Diodes (D2 Dual Package Common Cathode), 380 VDC Input, 20 V, 1 µs / div.

13.6 *Short-Circuit*

For tests shown below, the supply output was shorted with a mercury displacement relay at 100 W load, 380 VDC input. The oscilloscope was set to trigger on current rise.

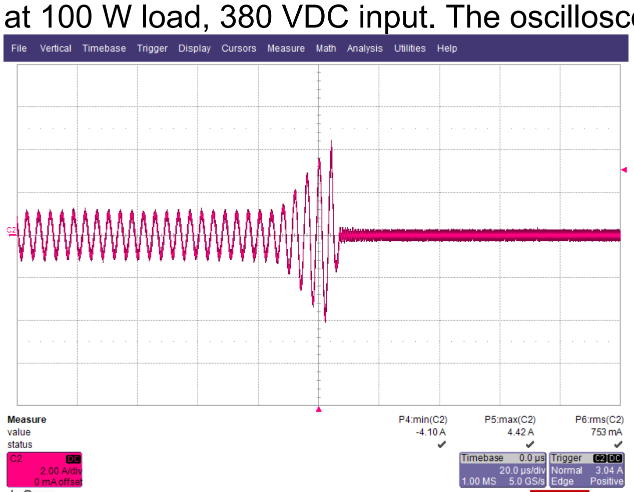

Figure 23 – Primary Current Waveform During 12 V Output Short-circuit, 2 A, 20 µs / div.

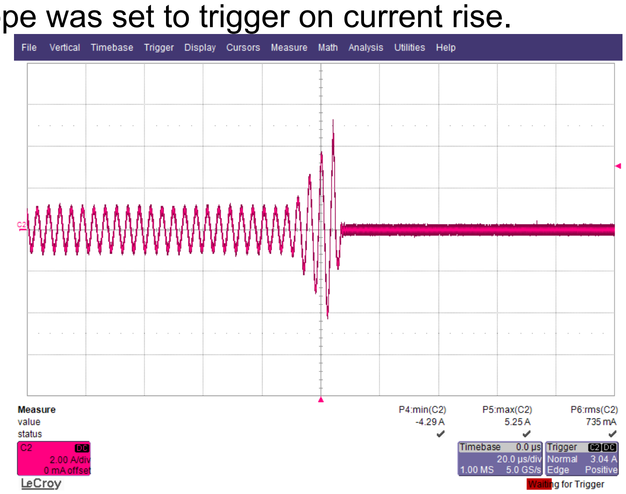

Figure 24 – Primary Current Waveform During 24 V Output Short-circuit, 2 A, 20 µs / div.

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13.7 Output Ripple Measurements

13.7.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

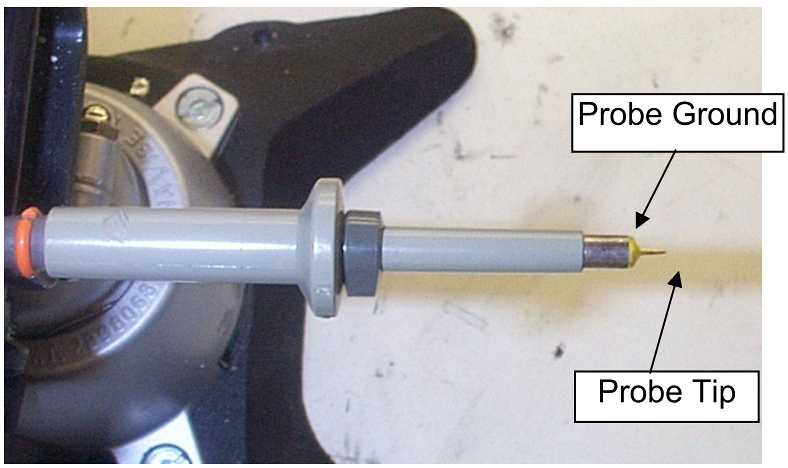

Figure 25 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

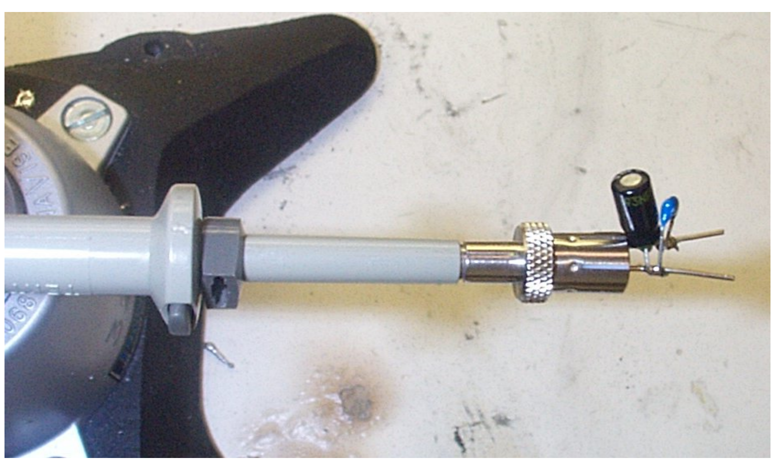

Figure 26 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

13.7.2 Output Ripple Measurement Results

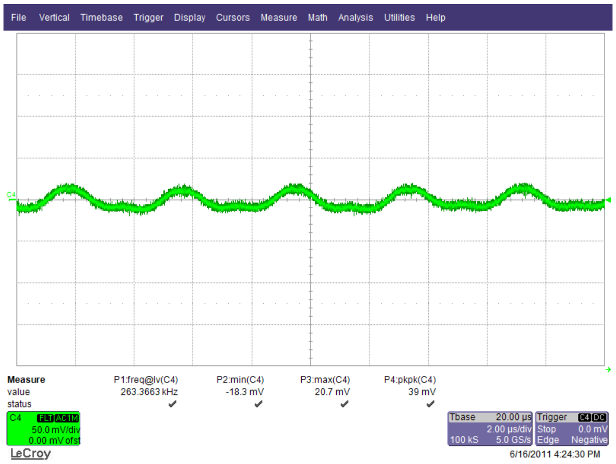

Figure 27 – 12 V_{RIPPLE}, 380 VDC, Full Load.
50 mV, 2 µs / div.

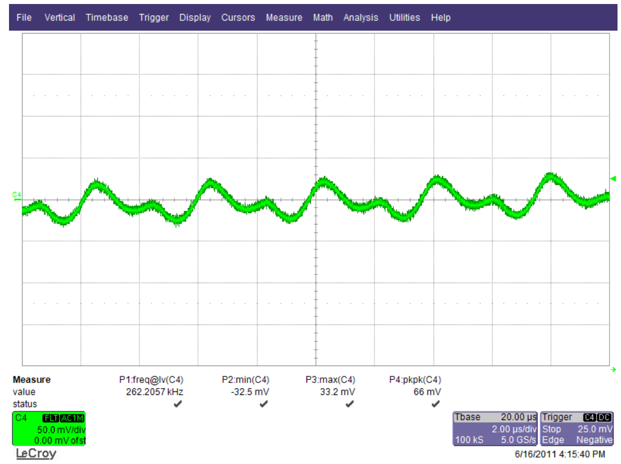

Figure 28 – 24 V_{RIPPLE}, 380 VDC, Full Load.
50 mV, 2 µs / div.

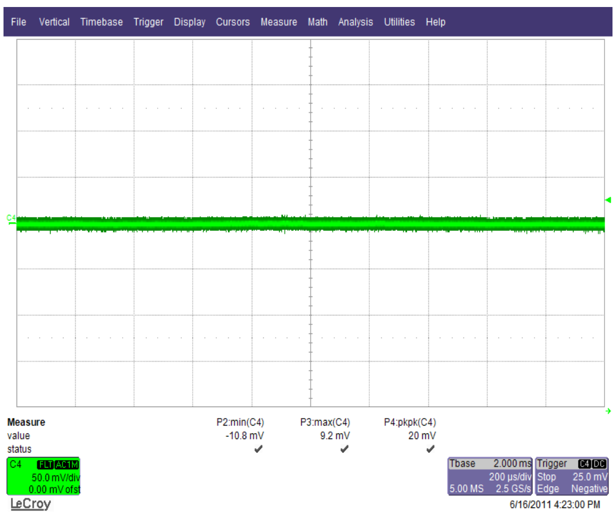

Figure 29 – 12 V_{RIPPLE}, 380 VDC, No-Load.
50 mV, 200 µs / div.
(Power Supply is not in Burst Mode.)

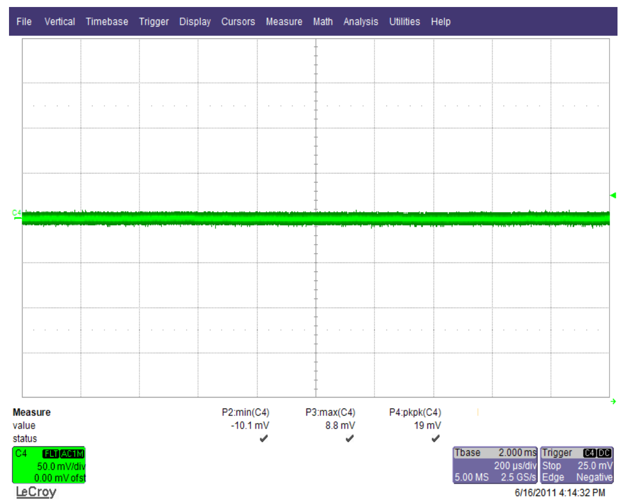

Figure 30 – 24 V_{RIPPLE}, 380 VDC, No-Load.
50 mV / div. 200 µs / div.
(Power Supply is not in Burst Mode.)

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14 Temperature Measurements

14.1 Conditions: 380 VDC, Full Load, 1 Hour Soak

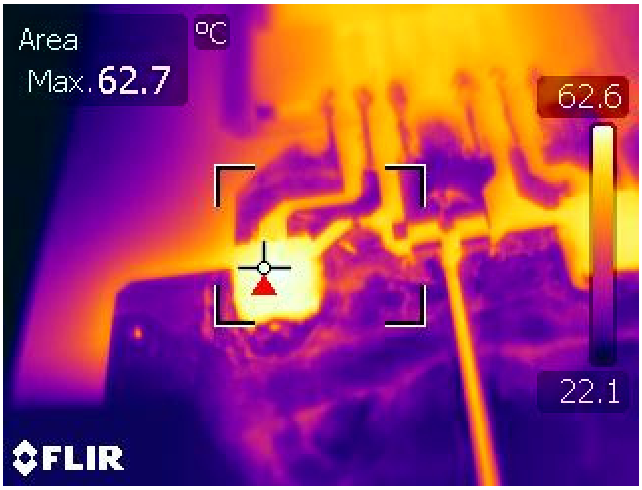

Figure 31 – Full Load 24 V Rectifiers (D2) Thermal Top View, Room Temperature.

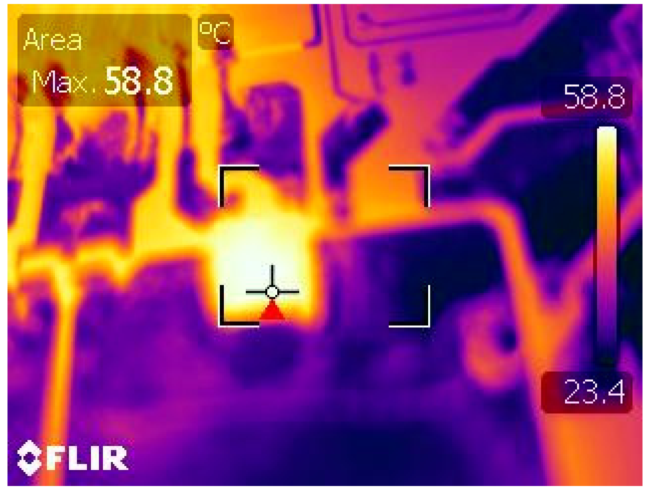

Figure 32 – Full Load 12 V Rectifiers (D3) Thermal Top View, Room Temperature.

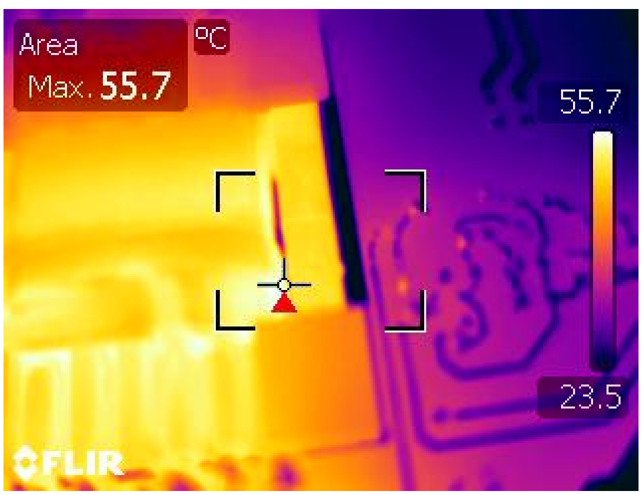

Figure 33 – Full Load Transformer (T1) Thermal View, Room Temperature.

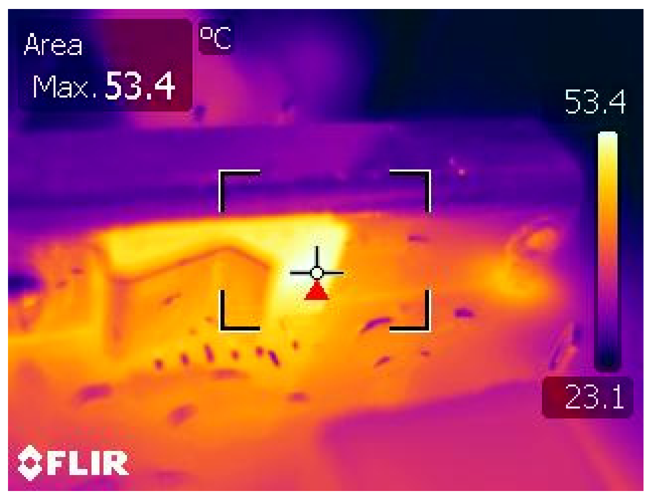

Figure 34 – Full Load HiperLCS (U1) Thermal View, Room Temperature.

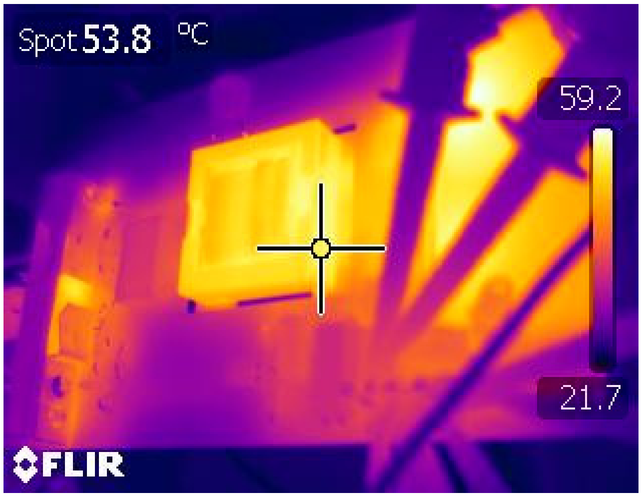

Figure 35 – Top Side of the Board.

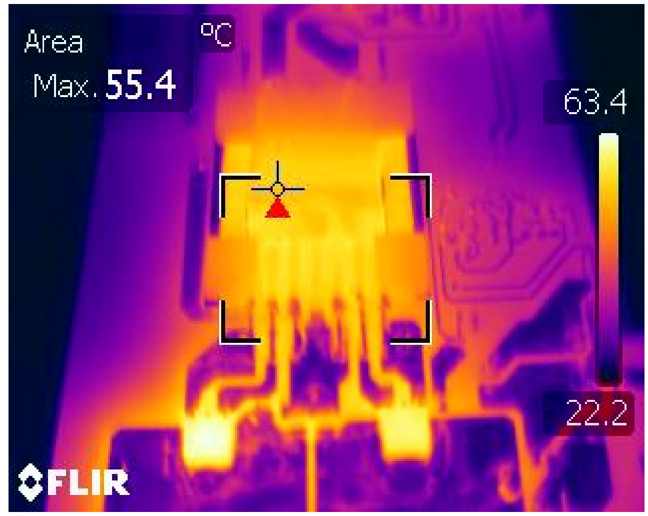

Figure 36 – Bottom Side of the Board.

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15 Revision History

Date	Author	Revision	Description and Changes	Reviewed
13-Sep-11	SS	1.2	Initial Release	Apps and Mktg

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